Conference Paper

A PWM Strategy for the Minimisation of Losses in a 3-level T-type Voltage Source Inverter

Anuchin, A., Shpak, D., Gulyaeva, M., Aliamkin, D., Zharkov, A., and Vagapov, Y.

This is a paper presented at the IEEE Int. Symp. on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Amalfi, Italy, 20-22 June 2018.

A PWM Strategy for the Minimisation of Losses in a 3-level T-type Voltage Source Inverter

Alecksey Anuchin
Department of Electric Drives
Moscow Power Engineering Institute
Moscow, Russia
anuchin.alecksey@gmail.com

Maria Gulyaeva
Department of Electric Drives
Moscow Power Engineering Institute
Moscow, Russia

Alexandr Zharkov
Department of Electric Drives
Moscow Power Engineering Institute
Moscow, Russia

Dmitry Shpak
Department of Electric Drives
Moscow Power Engineering Institute
Moscow, Russia

Dmitry Aliamkin
Department of Electric Drives
Moscow Power Engineering Institute
Moscow, Russia

Yuriy Vagapov
School of Applied Science, Computing and Engineering
Glyndwr University
Wrexham, UK
y.vagapov@glyndwr.ac.uk

***Abstract*—This paper discusses the approach for the witching loss minimisation in a 3-level inverter. It utilises a model predictive method which is used for evaluation of both the switching loss and voltage unbalance. The method is based on the cost functions implemented to provide simultaneous minimisation of loss and DC link voltage balance control. The simulation results shown that the total loss is reduced in 15% compared to a standard PWM strategy for a 3-level inverter operating at PWM frequency of 16 kHz.**

Keywords—Three-level inverter, PWM strategy, Switching losses minimisation, Predictive control, Voltage balance.

I. INTRODUCTION

In recent years, the area of industrial and domestic applications of 3-level inverters has been rapidly expanded. This is due to active support from manufacturers offering new power semiconductor modules which are specialised for implementation of a 3-level inverter topology in electrical power conversion installations. Nowadays, the applications of this topology include high-power and photovoltaic (PV) converters, uninterruptable power sources (UPS) and precision power supplies [1]-[3]. Compared to other power electronic topologies the 3-level inverter has the following well-known advantages:

- smaller voltage derivatives that results in longer life of motor insulation;
- less distortion in the output voltage due to smaller impact of a dead-time;
- smaller switching losses because of smaller commutating voltage;
- higher possible switching frequency and current loop passband correspondingly;
- decrease of weight and size of the output sine-filter (if it is used).

However, 3-level inverter topology requires a higher number of semiconductor switches which increases total cost of power electronic device due to increased number of power modules and gate driver circuits. It also requires two DC link voltage sensors in the system instead of a single one for the 2-level inverter.

Three-level inverters can operate under various pulse width modulation (PWM) strategies including space vector PWM (SVPWM). However, in order to provide reliable and efficient operation of a 3-level inverter the voltage balance of the input capacitors must be ensured. The 3-level inverter operation under negative or positive clamped discontinuous PWM (DPWM) does not provide the balance because one of the input capacitors is discharged. The unbalance of the DC link voltage across the capacitors can cause the breakdown of the inverter and/or the same capacitors. Thus, the change of clamping is required to limit the unbalance voltage rate of the capacitors to provide the safe operation [4].

A common problem related to all types of semiconductor converters is how to reduce and minimise the switching losses. As for 2-level inverters, there are several solutions aimed to reduce the loss which based on an appropriate selection of a DPWM switching pattern producing minimum switching losses [4-6]. There are always two options for positive and negative clamped DPWM where two different phases of the inverter remain in the same state during whole PWM cycle. The best option is the one where current is higher at that particular phase because there are no switching losses.

Although the decision about preferable clamping for 2-level inverter can be made using analysis of the absolute value of the phase current, this method can not be implemented in the same way for the 3-level inverter. The difference in the parameters of the switches for the AC switch part and bridge part of the inverter requires precise loss estimation including both switching and conductive losses. Moreover, 3-level inverter control may have up to 5 possible PWM patterns for the same referenced voltage vector depending on voltage magnitude and angle that makes the selection of the optimal PWM pattern even more complex. Some previously conducted researches [8] solved the problem but these solutions do not take into account

The research was performed with the support of the Russian Science Foundation grant (Project № 16-19-10618).

the difference in parameters of semiconductor switches for the AC and bridge inverter parts.

In this study both problems of loss minimisation and voltage balance are considered. It is suggested to implement predictive control approach to estimate the inverter losses for all possible solutions and to apply cost function which selects the best option to be implemented by the 3-level inverter. From the variety of the 3-level inverter topologies, the T-type inverter has been chosen for the further analysis. This topology has two bridge part switches for the full DC link voltage and two series-connected switches for half of the rated voltage in AC switch part. The circuit configuration of the considered inverter is shown in Fig. 1.

II. Space Vector Modulation for 3-level Voltage Source Inverter

In addition to positive and negative bus bar clamping, the 3-level inverter topology provides possible clamping of each phase to the neutral point or midpoint of the DC link capacitors. Fig. 2a shows all possible types of PWM patterns that can be implemented for various magnitudes of the output voltage. For instance, the depicted voltage vector can be implemented three different ways explained in Fig. 2b. It is possible to make positive and negative bus bar clamping, and make midpoint clamping for phase B. In case of midpoint clamping of phases A and C some reference voltages in other phases exceed the limits of the DC link [10].

Evaluation of the duty cycles for each case can be done for the referenced phase voltages v_a , v_b and v_c using the following sequence. At the first step, the voltage references for all cases should be evaluated:

$$\begin{bmatrix} v_a^N & v_a^P & v_a^A & v_a^B & v_a^C \\ v_b^N & v_b^P & v_b^A & v_b^B & v_b^C \\ v_c^N & v_c^P & v_c^A & v_c^B & v_c^C \end{bmatrix} = \begin{bmatrix} v_a & \dots & v_a \\ v_b & \dots & v_b \\ v_c & \dots & v_c \end{bmatrix} - \begin{bmatrix} \Delta v^N & \Delta v^P & \Delta v^A & \Delta v^B & \Delta v^C \\ \Delta v^N & \Delta v^P & \Delta v^A & \Delta v^B & \Delta v^C \\ \Delta v^N & \Delta v^P & \Delta v^A & \Delta v^B & \Delta v^C \end{bmatrix}, \quad (1)$$

where right part of the equation is the matrix with homopolar voltages corresponding to each PWM pattern. Its members are defined as following [8, 9]:

$$\left.\begin{aligned} \Delta v^N &= \min(v_a, v_b, v_c); \\ \Delta v^P &= \max(v_a, v_b, v_c); \\ \Delta v^A &= V_{CL} - v_a; \\ \Delta v^B &= V_{CL} - v_b; \\ \Delta v^C &= V_{CL} - v_c, \end{aligned}\right\} \quad (2)$$

where V_{CL} is the voltage of the bottom DC link capacitor.

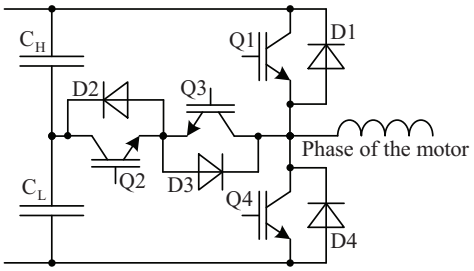

Fig. 1. Three-level inverter configuration (only one of three phases is shown).

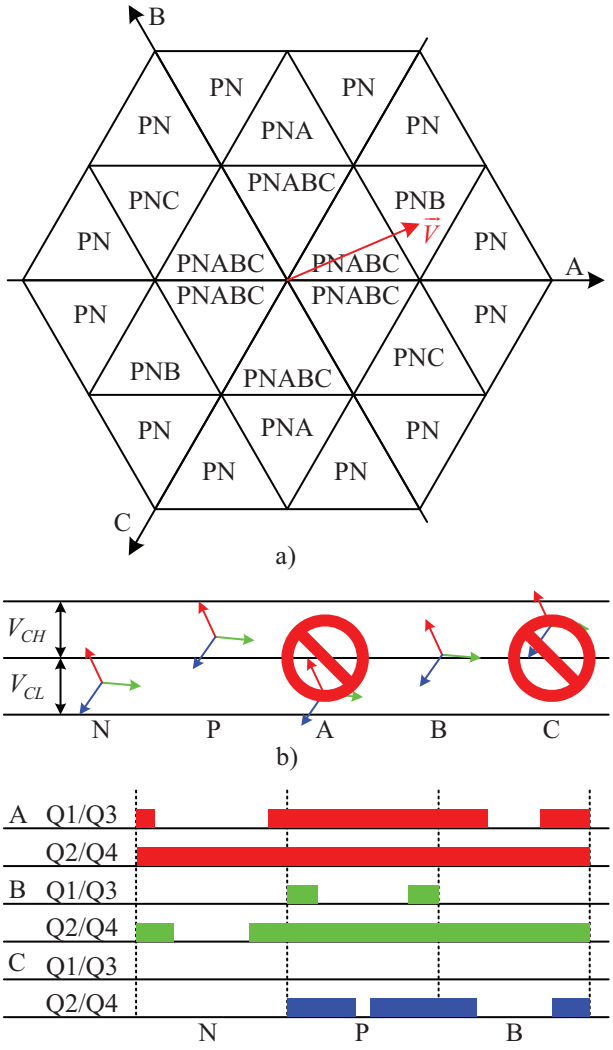

Fig. 2. Three-level inverter possible PWM patterns (a); examples of vector implementations (b); PWM patterns for each case (c).

After that stage the feasibility of each set of the voltage references has to be checked. Depending on the magnitude of the voltage vector, its angle, DC link voltage, and the distribution of the voltage between capacitors some sets of references should be discarded from the further consideration. This occurs when at least one of the reverences is smaller than zero or greater than DC link voltage.

At the next stage, the duty cycles for each voltage reference are to be evaluated:

$$\gamma_{Lj}^{i} = \begin{cases} \text{if } \left(v_j^i > V_{CL}\right), \text{ then 1;} \\ \text{else } \dfrac{v_j^i}{V_{CL}}, \end{cases}$$
$$\gamma_{Hj}^{i} = \begin{cases} \text{if } \left(v_j^i > V_{CL}\right), \text{ then } \dfrac{v_j^i - V_{CL}}{V_{CH}}; \\ \text{else 0,} \end{cases} \qquad (3)$$

where γ_{Lj}^{i} is the duty cycle for Q2 switch and γ_{Hj}^{i} is the duty cycle of Q1 switch. The Q3 switch operates complementary to Q1 and Q4 to Q2 respectively.

III. Losses Evaluation in 3-level Inverter

There are three types of losses which are considered for the inverter analysis:

- conducting losses caused by voltage drop in a switch and/or diode;
- losses occurred in a transistor during switching on and off;
- reverse recovery losses in a freewheeling diode.

A. Conducting Losses

The voltage drop across the switches and diodes depends on the duty cycles and the direction of the current flow. Consider the conditions where $\gamma_L = 1$ and $\gamma_H = (0;1)$. This means that the Q2 switch is always on and Q1 and Q3 switches are connected to C_H capacitor and operate as a conventional inverter leg as shown in Fig. 3. For this case the conducting losses occur in the Q1 switch during its conducting state, and in Q2 and D3 the rest of the time. Conducting losses in Q4 are absent:

$$\begin{aligned} \Delta P_{Q1}^{cond} &= \Delta \mathrm{v}_{\mathrm{BQ}}(i)\gamma i; \\ \Delta P_{D1}^{cond} &= 0; \\ \Delta P_{Q2}^{cond} &= \Delta \mathrm{v}_{\mathrm{ACQ}}(i)(1-\gamma) i; \\ \Delta P_{D2}^{cond} &= 0; \\ \Delta P_{Q3}^{cond} &= 0; \\ \Delta P_{D3}^{cond} &= \Delta \mathrm{v}_{\mathrm{ACD}}(i)(1-\gamma) i; \\ \Delta P_{Q4}^{cond} &= 0; \\ \Delta P_{D4}^{cond} &= 0, \end{aligned} \qquad (4)$$

where $\Delta \mathrm{v}_{\mathrm{BQ}}(i)$ is a function of voltage drop across the bridge part switch with respect to current, $\Delta \mathrm{v}_{\mathrm{ACQ}}(i)$ is a function of voltage drop across the AC part switch and $\Delta \mathrm{v}_{\mathrm{ACD}}(i)$ is a function of voltage drop across the AC part diode. The same equations are used for evaluation of conducting losses for other direction of current and duty cycles.

B. Switching Losses in the Switch

The switching losses is occurred due to commutation of the switch when it changes over its condition from on to off state during t_{on} time and from off to on state during t_{off} time. When the switch is closing during the commutation time t_{off} the voltage across the switch is rising whereas the current through the switch is falling. This produces a portion of heat energy dissipated in the semiconductor structure of the switch. The heat energy is also produced when the switch performs an opposite commutation during the time t_{on} where the voltage across the switch is falling and the current is rising. The amount of heat energy depends on many parameters such as commutated voltage and current, gate resistance and the duration of reverse recovery process in the freewheeling diode of the complementary switch. Under the assumption that the gate resistance is constant and the parameters of the diode are fixed, the switching loss energy can be expressed with respect to flowing current for the rated voltage level V_{rated}. Actually, the diode parameters are deviated following the temperature. This is why, in order to take the parameter deviation into account, the 2D lookup table should be used for the switching loss evaluation. However, this procedure can be a time consuming even for modern microcontrollers. In addition, the commutated voltage also impacts on losses value, but the relation is generally linear. In the example shown in Fig. 3 only switching losses in Q1 are presented:

$$\Delta P_{Q1}^{sw} = \left(\mathrm{E}_{\mathrm{Bon}}(i) + \mathrm{E}_{\mathrm{Boff}}(i)\right)\frac{V_{CH}}{V_{rated}} f_{PWM}, \qquad (5)$$

where $\mathrm{E}_{\mathrm{Bon}}(i)$ is the switch-on energy of the bridge part switch with respect to the flowing current, $\mathrm{E}_{\mathrm{Boff}}(i)$ is the switch-off energy, and f_{PWM} is the PWM frequency.

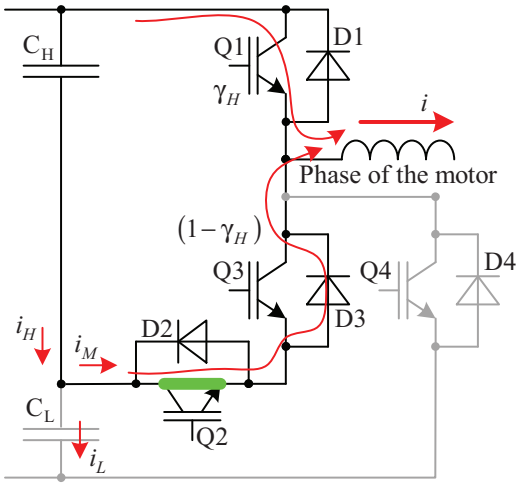

Fig. 3. Example of the current flow in 3-level inverter leg.

C. Reverse Recovery Losses

When Q1 is switching on, the diode D3 is conducting and the reverse recovery loss occur in D3. Theses losses depends on switching current, switching voltage and the gate resistance of the Q1 switch which defines the turn-on time. The losses can be evaluated as following:

$$\Delta P_{D3}^{RR} = \mathrm{E}_{\mathrm{Brr}}(i)\frac{V_{CH}}{V_{rated}} f_{PWM}, \tag{6}$$

where $\mathrm{E}_{\mathrm{Brr}}(i)$ is the reverse recovery energy as a function of the flowing current.

IV. Model of the Inverter

Inverter is represented with a zero-order hold which assumes that the voltage applied during entire PWM cycle and the current are constant. The PWM strategy should solve the problem of loss minimisation and perform voltage balancing at the input capacitors. The total midpoint current is the sum of all midpoint currents of each phase. The value of the midpoint current depends on the load current and duty cycles of high and low set of switches. For the configuration shown in Fig. 3 the load current flows through the midpoint when Q1 is off. Thus, the duration is defined by duty cycle of Q3. If the conditions are different: $\gamma_L = (0,1)$ and $\gamma_H = 0$, then the load current flows through the midpoint during the conductivity state of Q2. The universal equation is derived as follows:

$$i_M = i \cdot (1-\gamma_H)\gamma_L. \tag{7}$$

In its turn, midpoint current can be expressed via currents of the DC link capacitors which define the derivative of the midpoint voltage:

$$i_M = i_H - i_L = -C_H \frac{\mathrm{d}V_{CL}}{\mathrm{d}t} - C_L \frac{\mathrm{d}V_{CL}}{\mathrm{d}t} \tag{8}$$

Thus, both capacitor voltages can be expressed as:

$$\left.\begin{aligned} &\frac{\mathrm{d}V_{CL}}{\mathrm{d}t} = -(C_H + C_L)\cdot \sum_{j=a}^{c}\left(i_j \gamma_{Lj}\left(1-\gamma_{Hj}\right)\right); \\ &V_{CH} = V_{DC} - V_{CL}. \end{aligned}\right\} \tag{9}$$

V. Predictive PWM Strategy

The algorithm of PWM starts with computation of all five possible homopolar voltages according to (2) and then all five sets of the voltage references are evaluated by (1).

At the next stage, the feasibility of each set is to be checked according the following criterion: are any of the voltage references exceeds the DC link limits or not? After this stage, the sets which can be only implemented are left.

Then, the duty cycles are to be evaluated according to (3). This gives enough information for evaluation of the losses for all sets of the voltage reference left for this moment.

The computation of the losses is done according to the considerations given in the section III. Then, the total losses are evaluated as a sum of all partial losses. This gives from 2 to 5 values of losses, one value for each possible PWM pattern. The suggested cost function:

$$g = A \cdot \Delta\hat{P}_{\Sigma} + B \cdot R + C \cdot \left(\hat{V}_{CH} - \hat{V}_{CL}\right)^2, \tag{10}$$

where A, B and C are cost function weight coefficients, $\Delta\hat{P}_{\Sigma}$ is the estimation of total losses for the particular PWM pattern, R is reverse counter which counts down from the moment of last pattern change. If there is no change of the clamping, then it is equal to zero. If the clamping is different form the last one, then its value is considered in the equation and, in case of change, it is initialised with some constant value. The last component is the difference between estimated voltages of C_H and C_L capacitors.

VI. Simulation Results

The simulation was performed using Infineon F3L300R12PT4_B26, with 6600 uF capacitors in the DC link. Voltage reference is 220 V_{rms}, DC link voltage is 600 V, PWM frequency if 16 kHz, fundamental voltage frequency is 50 Hz.

The first simulation is done for the cost functions A and B equal to zero; C is set to 10. This test shows that the change of the PWM pattern occurs frequently in order to keep the voltages balanced all the time. This results in extra losses caused by extra switching during the clamping change. The total losses are 464.5 W.

Second simulation was performed with the cost function B equal to 200. Total losses were decreased down to 435 W. It has been observed that the voltage balance was on acceptable level whereas some states with clamping to midpoint were appeared (see Fig. 5).

Third simulation was performed when all the components of the cost function (10) are in consideration with A equal to 1. This operation mode gives 397 W of average losses (see Fig. 6).

It can be seen that the PWM patterns with midpoint clamping occurred very rear. This is caused by the particular parameters of the IGBT module. Also, the midpoint clamping is limited most of the time due to high magnitude of the output voltage. The test with a low magnitude of 110 V shows that the midpoint clamping occurs as can be seen in Fig. 7. Average losses are equal to 361 W.

The analysis of the midpoint clamping utilisation shows that this state is generally dictated by a voltage balance component of the cost function because each time, when these PWM patterns are chosen, the total losses are increasing. The same simulation with the value C = 1 (instead of 10) gives different shapes of duty cycles and the total loss of 333 W (see Fig. 8).

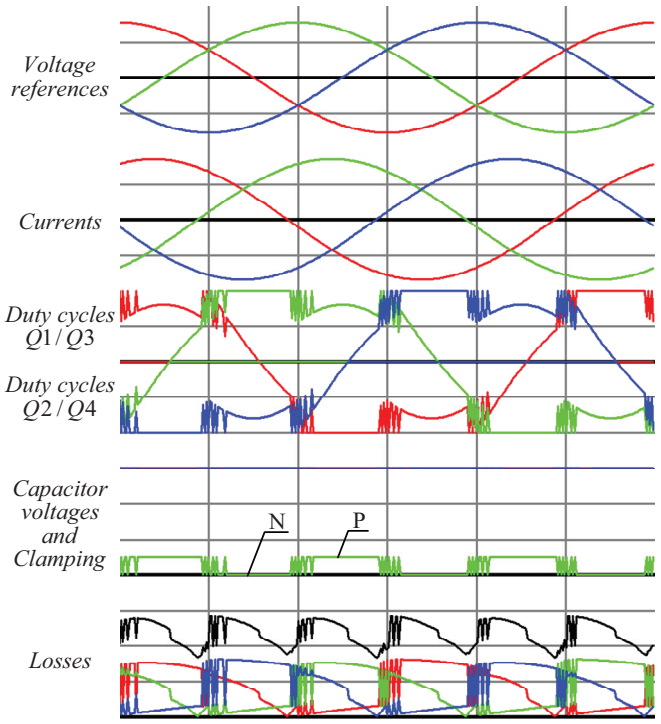

Fig. 4. PWM strategy with voltage balancing only (phase voltage — 200 V per division; current — 50 A per division; duty cycles — 50% per division; DC link capacitor voltage — 100 A per division; losses — 200 W per division; time — 3.33 ms per division).

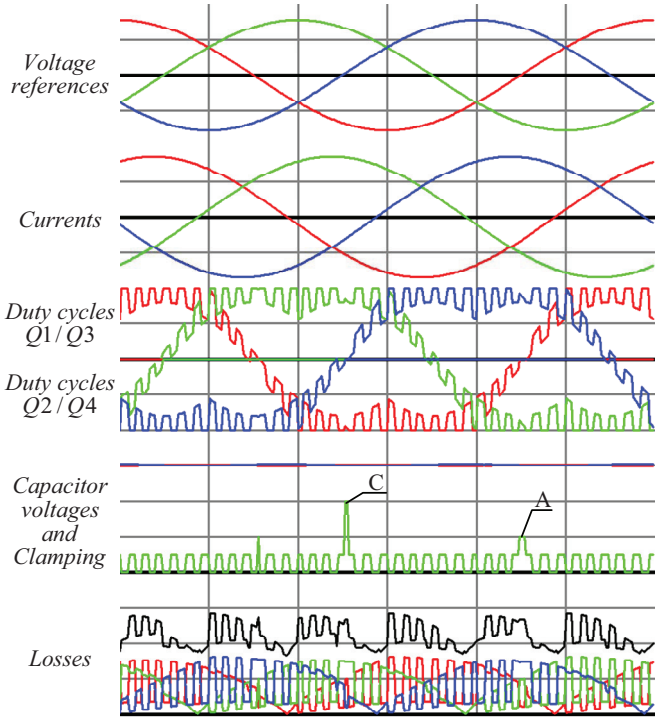

Fig. 5. PWM strategy with voltage balancing and limitation of clamping change frequency (phase voltage — 200 V per division; current — 50 A per division; duty cycles — 50% per division; DC link capacitor voltage — 100 A per division; losses — 200 W per division; time — 3.33 ms per division).

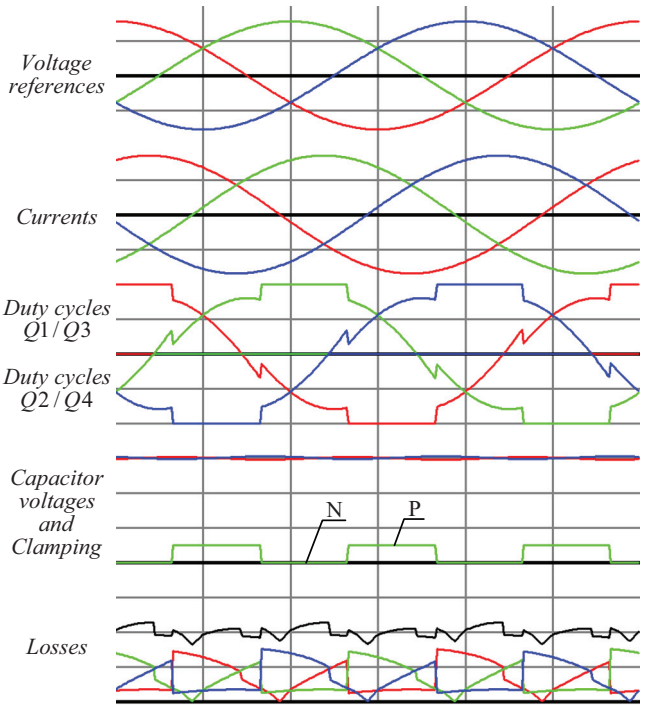

Fig. 6. PWM strategy with switching loss minimisation, voltage balancing and limitation of clamping change frequency (phase voltage — 200 V per division; current — 50 A per division; duty cycles — 50% per division; DC link capacitor voltage — 100 A per division; losses — 200 W per division; time — 3.33 ms per division).

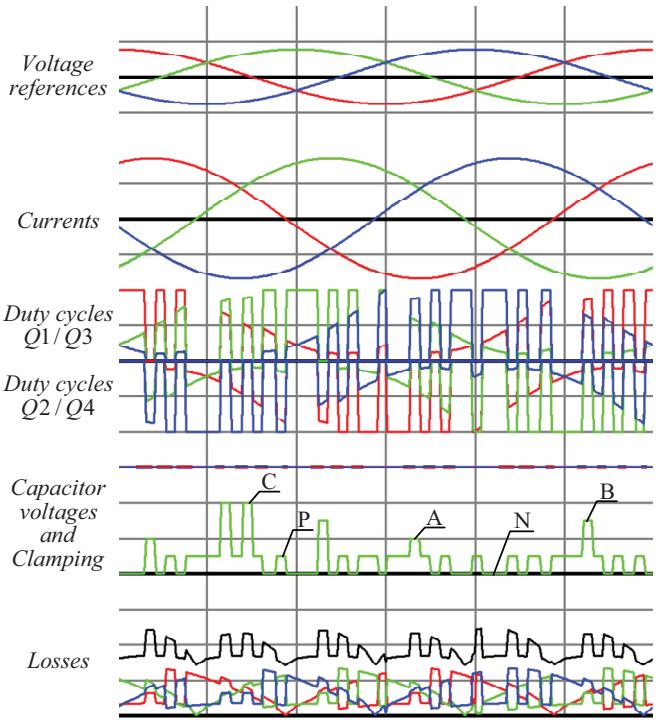

Fig. 7. PWM strategy with switching loss minimisation, voltage balancing and limitation of clamping change frequency (phase voltage — 200 V per division; current — 50 A per division; duty cycles — 50% per division; DC link capacitor voltage — 100 A per division; losses — 200 W per division; time — 3.33 ms per division).

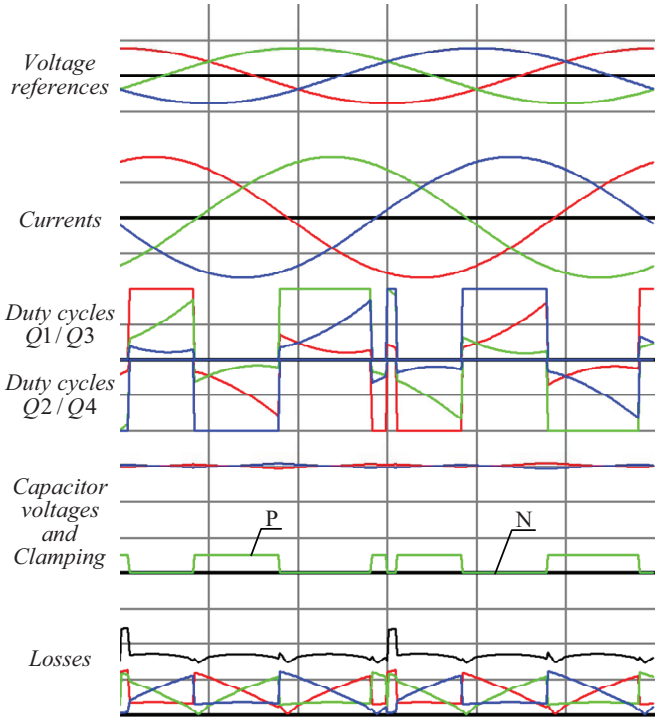

Fig. 8. PWM strategy with switching loss minimisation, voltage balancing and limitation of clamping change frequency (phase voltage — 200 V per division; current — 50 A per division; duty cycles — 50% per division; DC link capacitor voltage — 100 A per division; losses — 200 W per division; time — 3.33 ms per division).

VII. Conclusions

The proposed strategy for a 3-level inverter shows increase in the efficiency by 15% for the considered conditions. Due to complexity of the loss equation the model predictive method is the best option for the selection of the most efficient PWM pattern.

The experiments for the proposed solution were performed using the software model and in future investigations the tests using real hardware will be conducted.

References

[1] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. on Industrial Electronics*, vol. 57, no. 8, pp. 2581-2596, Aug. 2010.

[2] W.-T. Franke, N. Oestreich, and F.W. Fuchs, "Comparison of transformerless converter topologies for photovoltaic application concerning efficiency and mechanical volume," in *Proc. IEEE Int. Symp. on Industrial Electronics*, Bari, Italy, 4-7 July 2010, pp. 724-729.

[3] S. Ryvkin, R. Schmidt-Obermoeller, and A. Steimel, "Sliding-mode approach to control design for induction motor drive fed by a three-level voltage-source inverter," in *Proc. 13th Int. Power Electronics and Motion Control Conf. EPE-PEMC*, Poznan, Poland, 1-3 Sept. 2008, pp. 1505-1511.

[4] T. Bruckner, and D.G. Holmes, "Optimal pulse-width modulation for three-level inverters," *IEEE Trans. on Power Electronics*, vol. 20, no. 1, pp. 82-89, Jan. 2005.

[5] T. Kato, K. Inoue, Y. Taniyama, and K. Yamada, "Optimum reduction of switching losses based on the two-phase PWM modulation method for two-level inverter," in *Proc. 13th IEEE Workshop on Control and Modeling for Power Electronics COMPEL*, Kyoto, Japan, 10-13 June 2012, pp. 1-6.

[6] A.M. Hava, R.J. Kerkman, and T.A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. on Industry Applications*, vol. 34, no. 5, pp. 1059-1071, Sep.-Oct. 1998.

[7] M.C. Di Piazza, and M. Pucci, "Efficiency analysis in induction motor drives with discontinuous PWM and electrical loss minimization," in *Proc. Int. Conf. on Electrical Machines ICEM*, Berlin, Germany, 2-5 Sept. 2014, pp. 736-743.

[8] S. Calligaro, F. Pasut, R. Petrella, and A. Pevere, "Modulation techniques for three-phase three-level NPC inverters: A review and a novel solution for switching losses reduction and optimal neutral-point balancing in photovoltaic applications," in *Proc. 28th Annual IEEE Applied Power Electronics Conf. and Exposition APEC*, Long Beach, CA, USA, 17-21 March 2013, pp. 2997-3004.

[9] A. Anuchin, F. Briz, D. Shpak, and M. Lashkevich, "PWM strategy for 3-phase 2-level VSI with non-idealities compensation and switching losses minimization," in *Proc. IEEE Int. Electric Machines and Drives Conf. IEMDC*, Miami, FL, USA, 21-24 May 2017, pp. 1-6.

[10] S. K. Giri, S. Mukherjee, S. Kundu, S. Banerjee and C. Chakraborty, "An Improved PWM Scheme for Three-Level Inverter Extending Operation into Overmodulation Region with Neutral Point Voltage Balancing for Full Power Factor Range," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. PP, no. 99, pp. 1-12