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Design optimisation of air-forced heat sink to improve temperature gradient in power semiconductor modules

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ABSTRACT

This paper presents a numerical optimisation of an air-forced heat sink design for application in cooling systems for power electronic devices. A three-phase inverter is a typical power electronic circuit which commonly employs three or six power semiconductor modules installed in a row on an air-forced heat sink. When power loss is evenly distributed among the modules, the temperature increases along the heat sink in the direction from the air inlet to the outlet, creating a thermal gradient across the power semiconductors. This thermal gradient is a negative factor, leading to mechanical stress in the semiconductor structure and reducing the device's reliability and lifespan. To improve the temperature gradient, the study proposes a modification to the standard heat sink design by introducing a V-shaped cut in the fin area near the inlet. This modification creates an inconstant distribution of thermal resistance along the length of the heat sink reducing temperature variation. Numerical simulations were conducted to identify the optimal V-shaped cut configuration providing minimal temperature differences between modules. The optimal value of the V-shaped cut was determined to be 0.255pu, while the standard deviation of the temperature difference between the power semiconductor modules was reduced from 2.194 to 0.183 at a heat flux of 100W per module. The results show that the optimised design significantly reduces the thermal gradient, ensuring a more uniform temperature distribution across the semiconductor modules.

1. Introduction

Power semiconductors are key components of power electronic devices and systems, extensively used in a wide variety of industrial and domestic applications for energy conversion and processing. The operational reliability of such systems (e.g., electric drives, power supplies, renewable energy inverters, etc.) is significantly dependent on the failure performance of the power electronic components. Analysing the influence of semiconductors on the overall system reliability, Fischer et al. [1] reported that faults in power semiconductors constitute 13–18 % of total failures occurring in wind energy systems, whereas, according to Ref. [2], this figure rises to 31 % for power electronic converters used in other industrial applications.

The substantial impact on the reliability of the semiconductor components is related to the device temperature which follows the system's operating mode. The component temperature, and particularly its variation, is mainly responsible for the development of

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Symbols

C_p –	specific heat capacity [J/kg·K]
h –	heat transfer coefficient [W/(m^2·K)]
k –	thermal conductivity [W/m·K]
l –	depth of V-shaped cut [m]
L_h –	heat sink length [m]
n –	number of IGBT modules on the heat sink
p –	pressure [Pa]
q –	heat flux density [W/m^2]
Re –	Reynolds number
T_F –	fluid temperature [°C]
T_i –	average temperature of e i-th module [°C]
$T_{i,k}$ –	average surface temperature of i-th IGBT module for k-th mesh model [°C]
ΔT_k –	temperature difference for the k-th mesh model [°C]
u –	air velocity [m/s]
ε –	normalised V-shaped cut depth (per-unit of heat-sink length)
ε_{OPT} –	optimal normalised V-shaped cut depth
μ –	dynamic viscosity [Pa·s]
ρ –	air density [kg/m^3]
∇ –	gradient

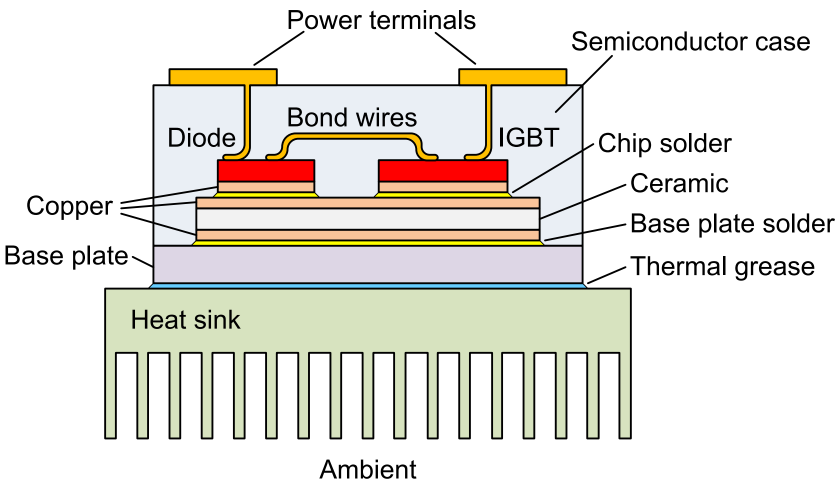

Fig. 1. Cross-section of a typical power semiconductor device consisting of an IGBT transistor and flywheel diode installed on the heat sink base.

thermal stress within the body of the semiconductor structure [3–7].

Thermal stress is a negative factor that significantly contributes to the reduction of semiconductor device reliability and lifetime. The thermal stress developed in the power semiconductor occurs due to differences in the thermal expansion of the materials composing the device structure. The stress initiates the mechanical fracture in the soldering and semiconductor layers, including the chip wire bonds. The further propagation of the thermomechanical fractures damages the device structure and leads to an unrecovered fault in the system [8–13].

There are three main factors affecting the thermal conditions of power semiconductors that can induce thermal stress development. These are (1) ambient temperature and (2) power loss in the semiconductor p-n junction reflecting the electronic system mission profile. Although both factors can produce temperature variation in a semiconductor structure, the second factor (power loss due to the mission profile) plays a major role in thermal cycling and, therefore, the occurrence of thermal stress [14–16]. The third important factor generating the thermal stress is (3) the temperature gradient across the semiconductor structure surface occurred due to nonhomogeneous heat transfer conditions or thermal resistance along the cooling system geometry or heat sink [17,18].

The vast majority of power electronic circuits designed for three-phase industrial converters consist of six IGBT-based electronic switches. Power semiconductor modules commonly used in such circuits typically integrate one or two IGBTs along with their corresponding free-wheel diodes into a single package. The heat generated in the module as a result of the power loss is concentrated in

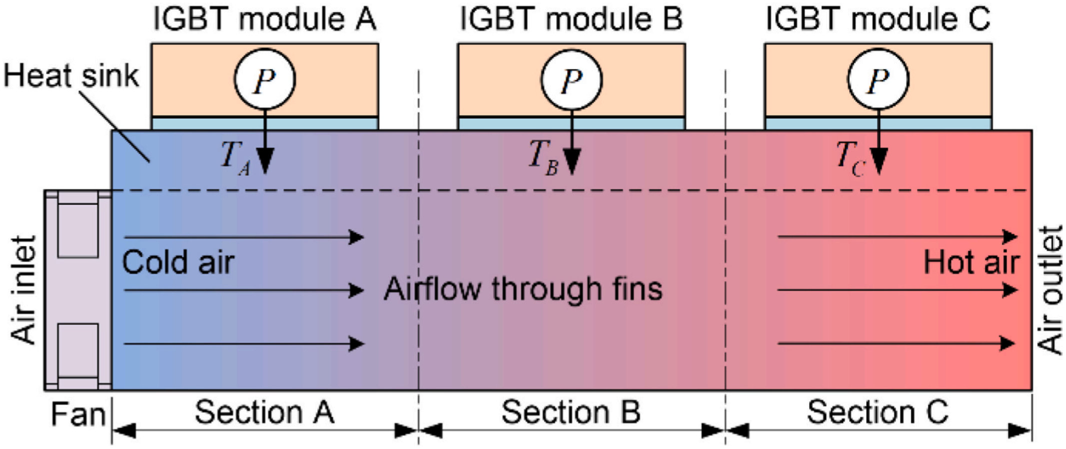

Fig. 2. Illustration of the thermal gradient development in a conventional air-forced heat sink; all IGBT modules have the same power loss P [W]; the temperature of the modules is increased from A to C ($T_A < T_B < T_C$).

both the IGBT and the flywheel diode and must be dissipated into the ambient environment through a heat sink. A typical cross-section of a power semiconductor device (IGBT transistor and flywheel diode) mounted on the top surface of the heat sink is illustrated in Fig. 1. The cross-sectional drawing shows that the device is composed of several layers of various materials (semiconductors, metals, ceramics, etc.) having different thermal expansion properties. Such a layered structure is susceptible to temperature gradients resulting from thermal cycling and nonhomogeneous cooling conditions. Today, in modern and advanced power semiconductor modules, the layout size of the IGBT and flywheel diode has been considerably increased to meet the higher rated power demands of the industry. The layered structure, having a larger square area, becomes more sensitive to the temperature gradient and more affected by thermal stress development [19–21].

A standard cooling solution commonly used in power electronic industrial applications is based on an air-forced heat sink, where the power semiconductor modules (three or six modules) are fixed on the heat sink surface in a "chain" arrangement. In this configuration, the semiconductors are placed in a single row aligned with the direction of airflow through the fins. The airflow, forced by a fan through the heat sink, provides an effective heat exchange from the heat sink fins to the ambient environment. However, the temperature of air travelling through the fin area from the airflow inlet to the outlet is gradually increased. This creates a thermal gradient along the length of the heat sink surface, resulting in different temperatures across the semiconductor modules. In particular, the hottest module is the last one in the "chain" at the heat sink outlet, whereas the coolest device is the module installed at the airflow inlet. Therefore, the difference in temperature between semiconductor modules reflects the thermal gradient that occurs in the cooling systems utilising a standard "off-the-shelf" air-forced heat sink. If the cooling system is modified in a way to reduce the temperature difference, it provides an improvement in the thermal gradient.

Fig. 2 illustrates the development of the thermal gradient in a standard air-forced heat sink implemented in a typical cooling system for three-phase power electronic inverter. Such a system is typically employed in electric drives, where the power losses in the semiconductor modules are assumed to be equal. This assumption is based on the fact that the inverter supplies a three-phase induction motor, representing a balanced electric load. The power loss imbalance caused by the implementation of standard space vector pulse width modulation (PWM) to control the power electronic circuit is considered negligible compared to other factors affecting loss distribution. These factors include mechanical and electrical asymmetries in the induction motor, device-to-device variations in conduction and switching characteristics, and nonuniformities in the thermal interface material used to mount the semiconductors to the heat sink. These variations are unpredictable and generally random, which leads to an almost equal power loss distribution among the semiconductor modules in practice.

A promising method for reducing the difference in the temperatures between power electronic semiconductors installed in a "chain" on a single heat sink is the active thermal control approach [22]. This method is based on modifying the standard space vector PWM and manipulating the PWM signals applied to control semiconductors to redistribute the power losses among the electronic components. The objectives of active thermal control in power electronic systems are typically both the semiconductor switching frequency and PWM duty cycle. These parameters affect conduction and switching power losses, which are the primary sources of heat generated by a semiconductor. An advantage of this method is that no hardware modification is required; this is a fully software-based solution implemented into the microcontroller operational code. For example, an attempt to implement the active thermal control approach for power loss redistribution in the three-phase inverter energising a switched reluctance electric drive is reported in Ref. [23]. The proposed thermal management strategy is based on a cost function algorithm utilising an electric drive model predictive control. Another active thermal control solution aimed at reducing the temperature difference among semiconductor components in an electric drive inverter is suggested in Ref. [24], where the semiconductors must be placed on the heat sink in a specific order according to the microcontroller software algorithm. However, active thermal control methods increase the total power loss and negatively impact the overall efficiency of the power electronic system.

Another option applicable for improving the thermal gradient is the specific design of a heat sink for a particular application, which

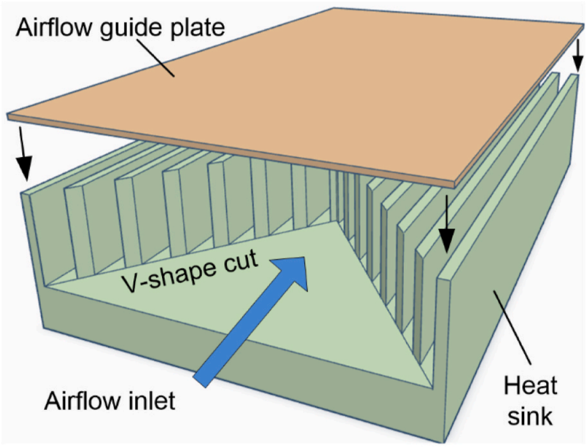

Fig. 3. Schematic illustration of the proposed V-shaped cut applied to a conventional air-forced heat sink. The drawing shows the bottom view of the heat sink; the power modules attached to the heat sink base surface are not visible.

can provide thermal resistance varying across the heat sink dimensions. The variable thermal resistance approach can be implemented in both natural and forced air cooling systems. Primarily, this solution aims to provide effective cooling of semiconductors that generate a nonhomogeneous heat flux over the device layout area. Such a heat sink usually has a complex shape that ensures variable thermal resistance, complementarily mapped to the non-uniform heat flux produced by the semiconductor [25–29]. For example, Al-Khamaiseh et al. [30] proposed a heat sink design for a high-power semiconductor that produced a non-uniform heat flux with higher heat density in the central area of the device layout. The proposed design is based on the variation of the fins' height across the heat sink dimensions to ensure appropriate thermal resistance. Therefore, the fins with the greatest height are installed in the areas generating the maximum value of the heat flux. Huang and Chen [31,32] suggested a similar solution; however, instead of variable-height fins, they proposed a variable "pin density" approach, where the number of square pins is increased in areas with the highest heat flux generation to improve thermal resistance. In general, specific heat sink designs having complicated geometry are considered quite advanced solutions but not cost-effective, particularly for mass production. It requires complex design and advanced manufacturing compared to conventional "off-the-shelf" heat sinks mass-produced by the electronics industry.

An interesting and cost-effective solution is proposed by Bunnagel et al. [33]. It suggests a simple and effective modification of the conventional heat sink cooling system, providing a uniform temperature distribution across the semiconductor devices installed on the surface of the heat sink in a single row. The advantage of the proposed solution is that the heat sink body itself is not modified; instead, a small alteration is made to the heat sink guide panel fixed to the bottom side of the heat sink to form channels alongside the fin area for air-forced cooling. According to the suggestion, a V shaped segment (V-cut) is removed from the guide panel. The implementation of the modified guide panel increases the air intake area of the heat sink compared to the outlet area. Therefore, the thermal resistance across the heat sink geometry is varied to ensure that the difference in temperature between the power semiconductor modules is reduced. The proposed modification provides better uniformity in the temperature distribution between the power electronic modules leading to significant improvements in the thermal gradient. However, in contrast to the ordinary cooling scheme, where the fans are installed at the inlet to blow air into the heat sink channels, this approach requires an unconventional fan installation: the fans must be attached to the outlet to extract air from the heat sink channels. This means that the fans, processing the hot air from the heat sink, operate at a considerably higher temperature. The increase in the fan temperature obviously impacts their lifetime and operational reliability. A similar disadvantage occurs in the cooling systems proposed by Fu et al. [34,35], where the fans are installed at the outlet to extract air from the heat sink and operate under high-temperature conditions.

This paper proposes a novel heat-sink design approach that improves thermal gradients in power semiconductors, thereby enhancing the reliability and lifetime of the devices. The approach is based on numerical optimisation of the heat sink geometry applied to a standard, "off-the-shelf" component designed for forced-air cooling systems. The heat sink selected for the numerical investigation is a commercially available design intended to accommodate three power semiconductor modules arranged in a single row, as required for a three-phase converter circuit. Through the proposed optimisation, the heat sink geometry is modified to reduce temperature differences across the power semiconductor modules and, therefore, to improve thermal uniformity along the length of the heat sink. The modification involves removing a section of the heat-sink fins in the form of a V-shaped cut using conventional machining processes, creating a controlled variation in thermal resistance along the airflow direction. The optimisation procedure identifies the optimal V-shaped cut configuration that minimises temperature non-uniformity. The modified heat sink retains a conventional fan installation at the air inlet, ensuring that the cooling fans operate under the same ambient conditions as in the standard design. The thermal performance of the optimised heat sink was evaluated through numerical simulations to determine the optimal geometric modification.

Accordingly, the objectives of this study are to: (1) quantify the influence of V-shaped cut depth on thermal performance by evaluating the standard deviation of module temperatures over a heat-flux range of 50W–100W per IGBT module; (2) identify the optimal V-shaped cut depth that minimises temperature non-uniformity; and (3) analyse airflow and static-pressure characteristics

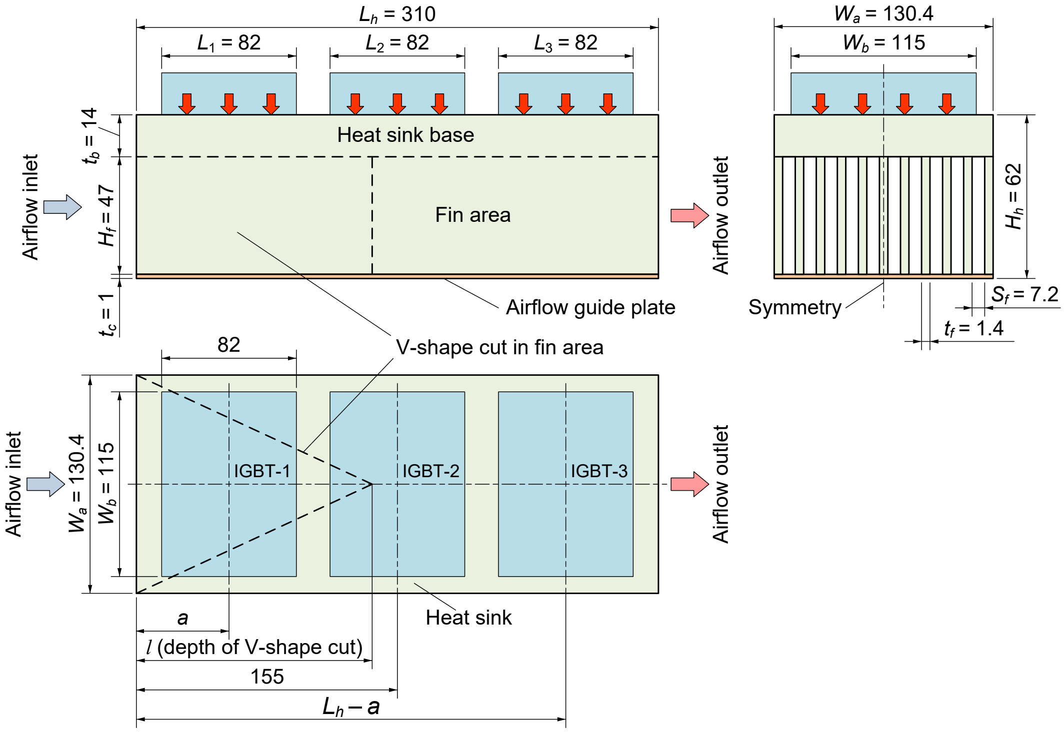

Fig. 4. Schematic drawing of the heat sink with dimensions (all dimensions are in mm).

associated with different V-shaped cut geometries to understand the aerodynamic effects of the modification and assess its applicability to standard off-the-shelf heat sinks.

2. Proposed approach

As mentioned above, a conventional heat sink with forced air cooling has three (or six) power semiconductors placed in a single row along the direction of air flowing through the fin area. This configuration causes a non-uniform temperature distribution between the semiconductors and produces a thermal gradient along the heat sink top area and the semiconductor base length (Fig. 2). To improve the thermal gradient and reduce the difference in the semiconductors' temperature, it is proposed to modify a standard heat sink by removing a section of the fins in the form of a V-shaped cut at the inlet side, as shown in Fig. 3. This is the only modification required to improve the thermal gradient performance of a standard "off-the-shelf" heat sink widely used in conventional air-forced cooling systems (no changes are needed to the fan installation or airflow guide plate). The shape of the cut is simple, requires only conventional cutting machinery, and can be implemented in electronic industry mass production.

The proposed design provides a non-uniform distribution of thermal resistance along the length of the modified heat sink. The heat sink section at the airflow intake has a smaller surface area for heat transfer and, therefore, higher thermal resistance compared to a conventional heat sink design. As a result of the increased thermal resistance in the area at the intake zone, the temperature rise of the air flowing through this section is reduced. In addition, this modification raises the temperature of the first semiconductor module (installed close to the air inlet) and partially raises the temperature of the middle module. Therefore, under the assumption that each device produces the same amount of power loss, the semiconductors achieve similar temperatures, significantly reducing the thermal gradient.

Obviously, the increase in the temperatures of the first and middle semiconductor devices can be considered a negative factor. However, modern high-power semiconductor devices are designed to operate at higher temperatures, while being quite sensitive to temperature swings and thermal gradients (particularly devices with a large semiconductor layout area) [19]. Therefore, the trade-off in the proposed design between increased temperatures in the power semiconductor modules and reduced thermal gradients is intentional and motivated by reliability considerations. Although the average temperatures of the first two modules increase, all modules remain well within their allowable operating temperature limits. The substantial reduction in temperature variation is expected to provide a net benefit in terms of device lifetime and reliability.

The advantage of the proposed design compared to Refs. [33–35] is that the fans are mounted at the airflow inlet, as in conventional air-forced cooling systems, and operate by blowing cold air into the heat sink. Hence, it can be used to modify existing heat sink based cooling systems designed and supplied by industrial electronic manufacturers.

The variation of the heat transfer conditions and, therefore, thermal resistance along the heat sink length is related to the depth of the V-shaped cut in the fin area. The optimisation criterion applied for the analysis is developed using the temperature difference between the power electronic modules. This criterion is considered the benchmark for the primary evaluation of the thermal gradient. The main objective of this optimisation study is to conduct an analysis of the temperature variation between the power electronic modules and to determine the optimal depth of the V-shaped cut that provides the lowest temperature difference between devices.

3. Numerical modelling and analysis

The V-shaped cut approach to improving the temperature gradient is verified through numerical analysis and simulations conducted using a standard heat sink I71 [36], selected for this investigation as an example of a typical "off-the-shelf" component. The heat sink I71 has dimensions (Width: 130.4 mm × Height: 57 mm × Length: 310 mm) and is designed to provide cooling for three IGBT power electronic modules CM400T-24S1 [37]. The modules are connected to form a three-phase ac inverter circuit energising an ac electric motor drive.

The manufacturer designed the IGBT modules with a metal base to be used for attachment to the heat sink surface. This design ensures efficient heat transfer through the metal base from the module case to the heat sink body. The size of the metal base for the selected device, which effectively serves as the heat flow generating area, is 115 mm × 82 mm. The modules are placed symmetrically with equal spacing and, assuming balanced inverter operation, experience the same power loss in each device. A set of model simulations was conducted under the condition that the power loss generated in each IGBT module varied in the range from 50W to 100W.

Fig. 4 shows the schematic drawing of the heat sink design used to build the numerical model employed for modelling and simulation. The drawing demonstrates the geometry and dimensional parameters of the heat sink I71 [36]. The exact installation of IGBT modules 1 and 3 is defined by the length a. This length is set to one-sixth of the total heat sink length ($a = 51.57$ mm), which represents the most common and recommended placement configuration for the majority of power electronic applications.

The schematic drawing in Fig. 4 also illustrates the configuration of the heat sink fin area, which was partially removed at the inlet to form a V-shaped cut (Fig. 3). The main parameter of the V-shaped cut is the altitude of the triangle fin-removed area obtained as a length perpendicular to the inlet side. The triangle altitude ε is expressed in pu, relative to the total length of the heat sink. Such normalisation of the V-shaped cut allows the proposed approach to be extended to other heat sinks with similar geometric configurations. For the simulation of the heat sink model, the parameter ε was varied in the range from 0 to 0.81 pu.

$$\varepsilon = \frac{l}{L_h} \tag{1}$$

where ε is the triangle altitude of the fin removed area in pu; l is the depth of the V-shaped cut in mm; L_h is the heat sink length ($L_h =$ 310 mm).

The conventional heat sink geometry without a V cut in the fin area ($\varepsilon = 0$) represents a reference model used to obtain the reference values for the benchmarking. According to the conventional configuration, the fans installed at the inlet blow air into the heat sink, producing forced airflow along the fins to enable convective heat transfer. Following the heat sink manufacturer's recommendations, the velocity of the airflow at the inlet is set to a standard value of 5 m/s [36].

In this study, the standard k–ε RANS turbulence model was used because plate-fin heat sinks operating at moderate Reynolds numbers (around $\mathrm{Re} \approx 5 \times 10^4$ for a 5 m/s inlet velocity) have fully turbulent, channel-dominated airflow. In such cases, the k–ε model provides stable and computationally efficient predictions of velocity and heat transfer behaviour. Although small local effects (secondary vortices, mild recirculation, or boundary-layer redevelopment near the fin entrances or around the V-shaped cut) can occur, these have only a minor influence on the average temperatures of the semiconductor modules, which is used for optimisation procedure. Since the optimisation compares relative temperature differences across the power electronic modules using standard deviation, rather than the absolute temperature prediction, the standard k–ε model is adequate for capturing the correct trends and the length of the optimal V-shaped cut. Therefore, the k–ε model offers a reliable and computationally robust basis for the optimisation results presented.

Modelling and numerical investigation of the proposed heat sink configuration were conducted employing ANSYS 2020 R2 Workbench Package. The 3-D models required for analysis were created using the ANSYS DesignModeler application and then proceeded to ANSYS Meshing. The computer hardware used for all numerical simulations was a custom-made PC workstation operating with the processor AMD Ryzen 9 5950X 16-Core and RAM of 128 GB.

3.1. Governing equations

Following the numerical approach to heat sink modelling proposed in Ref. [33], the airflow condition is defined using Reynolds number calculated as follows.

$$\mathrm{Re}_L = \frac{\rho u L}{\mu} \tag{2}$$

where ρ is the density; u is the velocity; L is the length of the heat sink; μ is the dynamic viscosity.

According to the condition that $\mathrm{Re}_L > 2300$, the k-epsilon turbulence model is selected for the simulation processing in ANSYS Fluent solver. Therefore, the numerical modelling of the heat sink utilises the governing equations listed below.

The continuity equation is defined as:

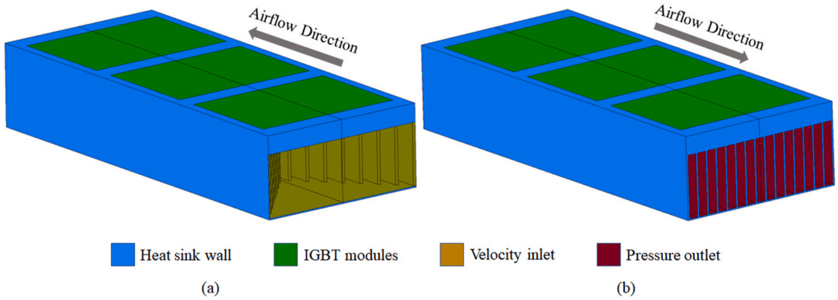

Fig. 5. Schematic illustration of boundary conditions in the numerical model: (a) front view and (b) rear view.

$$\nabla \cdot (\rho u) = 0 \tag{3}$$

where ∇ is the gradient.

The momentum equation is defined as:

$$\nabla \cdot (\rho uu) = -\nabla p + \mu \nabla^2 u \tag{4}$$

where p is the pressure.

The energy equation for the fluid domain is defined as:

$$\nabla \cdot \left(\rho u C_p T\right) = k \nabla^2 T \tag{5}$$

where C_p is the specific heat capacity; T is the temperature; k is the thermal conductivity.

The energy equation for the solid domain is defined as:

$$\nabla^2 T = 0 \tag{6}$$

The heat flux at the surface is defined as follows:

$$-k\nabla T = q \tag{7}$$

where q is the heat flux density.

The convection at the surface is defined as follows:

$$-k\nabla T = h(T_F - T) \tag{8}$$

where h is the heat transfer coefficient; T_F is the fluid temperature.

The symmetry condition is defined as follows:

$$-k\nabla T|_{x=C_L} = 0 \tag{9}$$

where C_L is the centre line.

3.2. Model boundary conditions

The schematic drawing in Fig. 4 shows that the heat sink's geometrical configuration is symmetrical. Therefore, only one symmetrical section of the heat sink is used for modelling to reduce the processing time required for the simulation by the ANSYS Fluent solver. The other section of the heat sink is then symmetrically replicated to build the full model. The set of numerical models is analysed with respect to the triangle altitude of V-shaped cut ε used as a parametric function for the optimisation.

The boundary conditions employed in the symmetrical model are shown in Fig. 5. Aluminium is selected for the heat sink material. Considering the fluid flow, the properties of air as the surrounding ambient, are chosen for the airflow region. Heat generated in the power semiconductors is transferred from the heat sink to the ambient by convection through the heat sink's surrounding surfaces (walls). A heat flux representing the heat dissipation from the modules is applied to the heat sink surface area corresponding to the layout of each IGBT module. To simplify the model, symmetry is applied to all solid and fluid surfaces at the domain's central faces. Air is blown into the heat sink through the air inlet (velocity inlet) at a speed of 5 m/s. The airflow at the inlet travels following the positive x-axes direction in accordance with the model axis arrangement. The air exits the model at the air outlet (pressure outlet), where atmospheric pressure is applied as the boundary condition.

3.3. ANSYS fluent solver settings

To conduct the simulations, the solver in ANSYS Fluent has been set up as follows: The double-precision option is selected for the

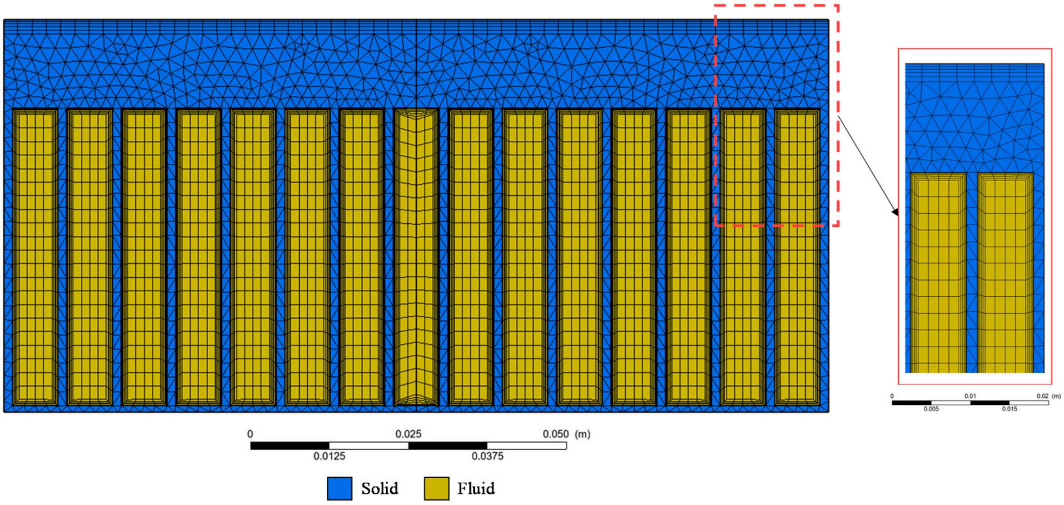

Fig. 6. Front view of the mesh elements distribution in the heat sink numerical model.

Table 1
Temperatures at the surface of IGBT modules (average values) for the mesh sensitivity analysis.

Mesh Model	Number of Mesh Elements	Temperature of Power Semiconductor Modules		
		IGBT-1	IGBT-2	IGBT-3
M1	153,039	59 °C	62.92 °C	64.34 °C
M2	232,132	59.02 °C	62.95 °C	64.37 °C
M3	470,081	59.30 °C	63.10 °C	64.48 °C
M4	653,056	59.45 °C	63.21 °C	64.57 °C
M5	885,884	59.44 °C	63.25 °C	64.63 °C
M6	1,120,902	59.46 °C	63.24 °C	64.60 °C

pressure-based solver, and the pressure-velocity coupling is set to the coupled algorithm. The least-squares cell-based method is applied to compute the gradient, while the pressure is discretised employing the second-order momentum scheme.

For turbulence modelling, the first-order upwind scheme is used to solve the turbulent kinetic energy and dissipation rate. Both the momentum and energy equations are discretised following the second-order upwind scheme.

To ensure precise and accurate results during the simulation, the threshold of 10^{-6} is selected as the absolute convergence criterion for residual values in all respective equations. For convection transfer applied to all external surface areas, the coefficient is based on the values provided by Mueller et al. [38]. The material properties of aluminium, including its thermal conductivity and specific heat, have been selected from the data provided by Fischer et al. [39]. The temperature of the ambient (air) is set to 24.85 °C, representing conventional environmental conditions.

3.4. Mesh sensitivity study

Mesh generation is an important stage of numerical modelling that impacts both the accuracy and efficiency of the simulation procedure. The mesh sensitivity study focuses on determining the appropriate mesh size and mesh model, ensuring a balance between the accuracy and complexity of the model. A heat sink configuration without a V-shaped cut and with maximum power loss in each IGBT module (heat flux of 100W) is selected for the mesh sensitivity study.

Six mesh models, with global element sizes ranging from 1 mm to 5 mm, are analysed to determine the best option for the simulation. The multizone meshing technique is employed using a hexa-mapped mesh type for the fluid domain, which represents the air surrounding the heat sink. A tetrahedral mesh is used for the solid domain representing the metal body of the heat sink to accommodate its complex geometry (see Fig. 6). Due to the intensive heat transfer from the IGBT modules to the heat sink, a more refined calculation structure of this area is required to ensure more accurate results. Therefore, the meshing of the metal body is inflated near the heat sink surface where three IGBT modules are installed. The IGBT module layouts act as the boundary layer (green area in Fig. 5). This refinement achieved through inflation is set up with an option “Maximum Layer” of 10 and a growth rate of 1.05.

Table 1 presents the results of the mesh sensitivity analysis conducted on six mesh models. These results are used to calculate the net surface temperature difference ΔT, which is proposed as the selection criterion for determining the best mesh model. The net surface temperature difference for each mesh model is calculated using the following formula.

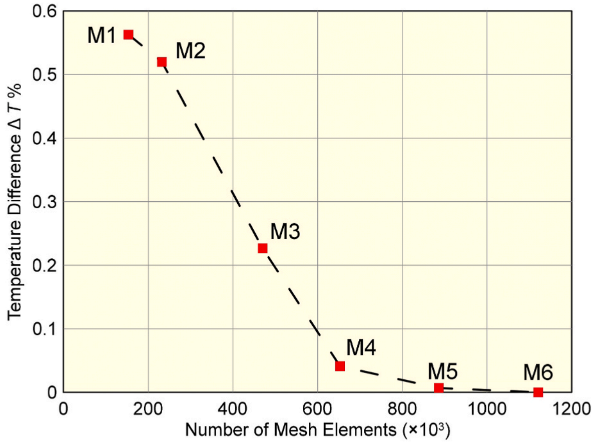

Fig. 7. Mesh sensitivity analysis. The temperature difference is expressed in % in comparison to the mesh model M6 (1,120,902 mesh elements). The mech model M5 (885,884 mesh elements) is selected as suitable for the numerical simulation.

$$\Delta T_k = \left| \frac{\sum_{i=1}^{n} T_{i,k} - \sum_{i=1}^{n} T_{i,6}}{\sum_{i=1}^{n} T_{i,6}} \right| \times 100\% \tag{10}$$

where ΔT_k is the temperature difference (in %) for the k-th mesh model, $T_{i,k}$ is the average surface temperature of i-th IGBT module for the k-th mesh model, n is the number of IGBT modules on the heat sink ($n = 3$).

Fig. 7 visualises the results obtained from the mech model criterion calculation, where the net surface temperature difference ΔT expressed in % is plotted against the number of mesh elements. Red symbols indicate the mesh models associated with their respective number of mesh elements. The plot shows that the net surface temperature difference values of the IGBT modules seem to be stabilised around 885,884 elements. Based on the data shown in Table 1, the temperature variation across the two finest meshes (M5 and M6) is approximately ± 0.03 °C. Therefore, model M5 appears to be the most suitable mesh configuration for this study, as it provides similar results compared to M6 but with fewer elements. Consequently, the mesh model M5 is selected for the simulations performed to analyse the proposed heat sink approach and conduct the geometry optimisation.

3.5. Optimisation of V-shaped cut

The thermal gradient across the semiconductor layout area (the area of the module metal base) in cooling systems equipped with conventional heat sinks significantly depends on the difference in the temperature of the power semiconductor modules. Reducing this temperature difference improves the thermal gradient within the semiconductor structures. Therefore, since the temperature difference is directly linked to the thermal gradient across the semiconductor layout, it can serve as an indirect criterion for predicting the thermal gradient condition in the semiconductor structure. Consequently, to achieve the best possible temperature gradient, the temperatures of the power electronic modules mounted on the heat-sink surface should differ as little as possible. As the parameter ε influences the net temperature of the semiconductor modules, it is possible to determine its optimum value corresponding to the minimum achievable thermal gradient across the semiconductor structure.

To develop the criterion of optimisation for the parameter ε, the standard deviation (SD) method is applied. This approach means that the minimum value of the standard deviation of the module temperatures corresponds to the optimum cut depth ε_{OPT} (in pu), at which the thermal gradient on the heat sink surface and within the IGBT modules is minimal. Therefore, the optimisation formula used to determine the best heat sink geometry is expressed as follows:

$$\min \sqrt{\frac{1}{n} \sum_{i=1}^{n} (T_i - T^a)^2} \rightarrow \varepsilon_{OPT} \tag{11}$$

where $T^a = \frac{1}{n} \sum_{i=1}^{n} T_i$ is the average temperature of n power electronic modules; T_i is the average temperature of the i-th module; n is the number of modules ($n = 3$ or $n = 6$, typical values for most power electronic converters for three-phase applications).

4. Results and discussion

The original heat sink designed and produced by the manufacturer was investigated as a benchmark model. The benchmark model has a full set of fins (no V-shaped cut implemented) corresponding to the parameter $\varepsilon = 0$. The temperatures of the IGBT modules obtained from this benchmark were used to establish reference values for evaluating and comparing the performance of the modified

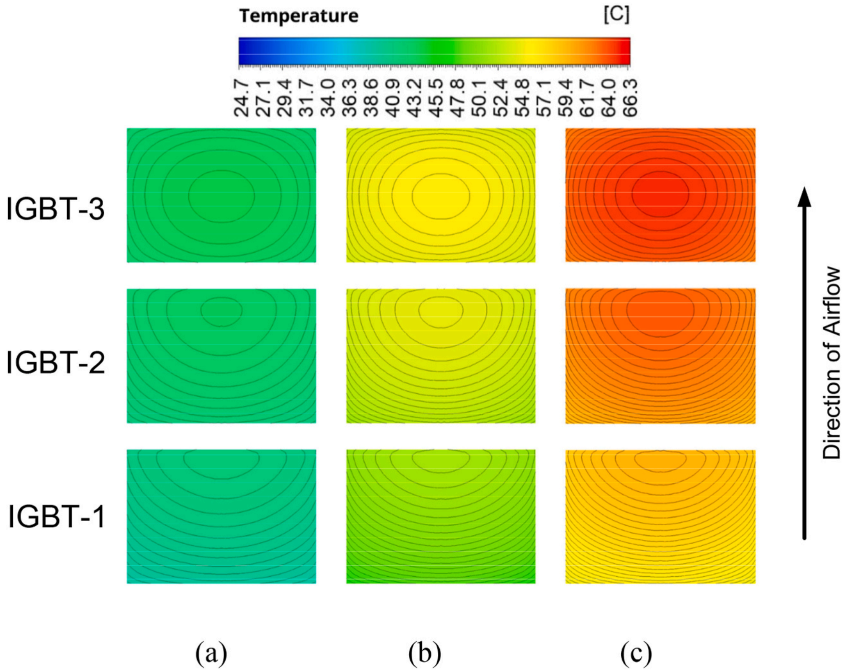

Fig. 8. Temperature distribution showing thermal gradient development within the IGBTs' surface in the benchmark model. Heat flux per IGBT module: (a) 50W; (b) 80W; (c) 100W.

Table 2
Comparison of the benchmark model ($\varepsilon = 0$) and the optimised V-shaped cut model ($\varepsilon = 0.255$pu).

Heat flux per IGBT module	Temperature on the metal base of IGBT modules (average values)							
	$\varepsilon = 0$ (benchmark model)				$\varepsilon = 0.255$pu (optimum value)			
	IGBT-1	IGBT-2	IGBT-3	StDev	IGBT-1	IGBT-2	IGBT-3	StDev
50W	42.15 °C	44.05 °C	44.74 °C	1.098	44.61 °C	44.45 °C	44.67 °C	0.094
60W	45.60 °C	47.89 °C	48.72 °C	1.317	48.55 °C	48.36 °C	48.63 °C	0.113
70W	49.06 °C	51.73 °C	52.69 °C	1.536	52.5 °C	52.28 °C	52.58 °C	0.129
80W	52.53 °C	55.58 °C	56.67 °C	1.754	56.44 °C	56.18 °C	56.55 °C	0.152
90W	55.98 °C	59.41 °C	60.65 °C	1.974	60.4 °C	60.1 °C	60.5 °C	0.17
100W	59.44 °C	63.25 °C	64.63 °C	2.194	64.34 °C	64.02 °C	64.46 °C	0.183

heat sink design. The non-uniform temperature distribution occurred within the surface area of the power semiconductor modules mounted on the benchmark heat sink is illustrated in Fig. 8 for three heat flux values per IGBT module: 50W, 80W, and 100W. These results show a significant temperature gradient development within the surface (metal base) area of the modules attached to the heat sink. The temperature performance data of the benchmark model ($\varepsilon = 0$) of the heat sink are summarised in Table 2.

The heat sink numerical model, modified according to the proposed approach, was investigated using six different V-shaped cuts in the fin area. The cut lengths (parameter ε, pu) selected for the analysis were as follows: ($\varepsilon = 0.184$ pu, $\varepsilon = 0.31$ pu, $\varepsilon = 0.437$ pu, $\varepsilon = 0.563$ pu, $\varepsilon = 0.69$ pu, $\varepsilon = 0.816$ pu). The plots of the average surface temperature distribution for the three IGBT modules versus different V-shaped cuts, including the benchmark model ($\varepsilon = 0$), are shown in Fig. 9. These plots visualise data obtained from the numerical simulations for three heat flux values per module (50 W, 80 W, and 100 W) corresponding to the results in Fig. 8. More detailed analysis is shown in Fig. 10, where the average surface temperature distribution is plotted for a narrower range of ε values (from 0.2 to 0.3) to determine the optimal V-shaped cut. For the detailed analysis, the model was investigated using six V-shaped cut lengths ($\varepsilon = 0.202$ pu, $\varepsilon = 0.22$ pu, $\varepsilon = 0.238$ pu, $\varepsilon = 0.256$ pu, $\varepsilon = 0.274$ pu, $\varepsilon = 0.292$ pu) for three heat flux values per module (50 W, 80 W, and 100 W). The plotted results in Fig. 10 clearly indicate that the optimal V-shaped cut length is $\varepsilon_{OPT} = 0.255$pu.

The optimal length ε_{OPT} corresponds to the lowest value of the standard deviation of the average temperatures in the power semiconductor modules. The standard deviation data for the optimal cut length are presented in Table 2. These results show that the optimal V-shaped cut is independent of the heat flux generated by the power modules due to power loss in the semiconductor structure. Although the temperatures of IGBT-1 and IGBT-2 are increased as a result of the degradation of the thermal resistance near the airflow inlet, the temperature differences between the modules become negligible compared to the benchmark model. In addition, the hottest IGBT module demonstrates a slight temperature reduction (by a fraction of a degree), which contributes to the partial improvement in

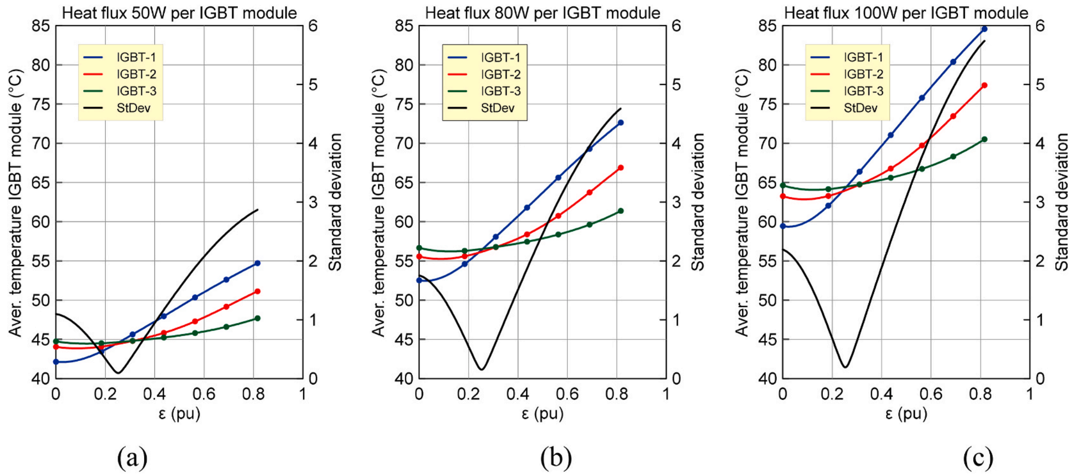

Fig. 9. Average temperature on the modules' surface and standard temperature deviation vs. V-shaped cut length ε in pu ($\varepsilon = 0$–0.81pu) for the three different heat flux per IGBT module: (a) 50W, (b) 80W, (c) 100W.

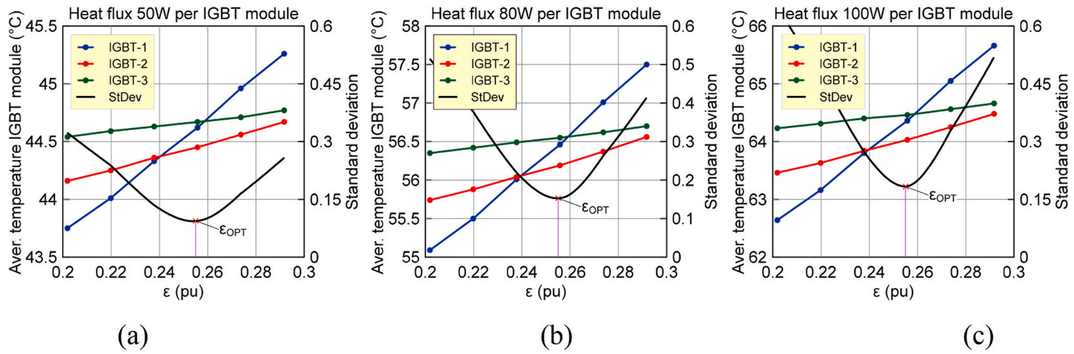

Fig. 10. Average temperature on the modules' surface and standard temperature deviation vs. V-shaped cut length ε in pu ($\varepsilon = 0.2$–0.3pu) for the three different heat flux per IGBT module: (a) 50W, (b) 80W, (c) 100W. The optimum parameter $\varepsilon_{OPT} = 0.255$pu.

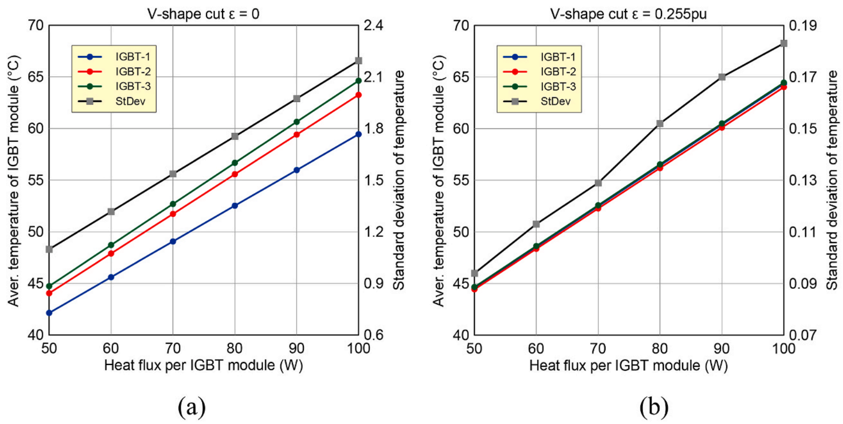

Fig. 11. The temperature distribution between IGBT modules and standard temperature deviation vs. heat flux per IGBT module: (a) benchmark model (no V-shaped cut, $\varepsilon = 0$); (b) model with optimal V-shaped cut ($\varepsilon = 0.255$pu).

the semiconductor reliability and, consequently, slightly enhances the overall performance of the power electronic system. The data in Table 2 are visualised in Fig. 11 showing average module temperatures and standard deviations for both benchmark design and optimised heat sink.

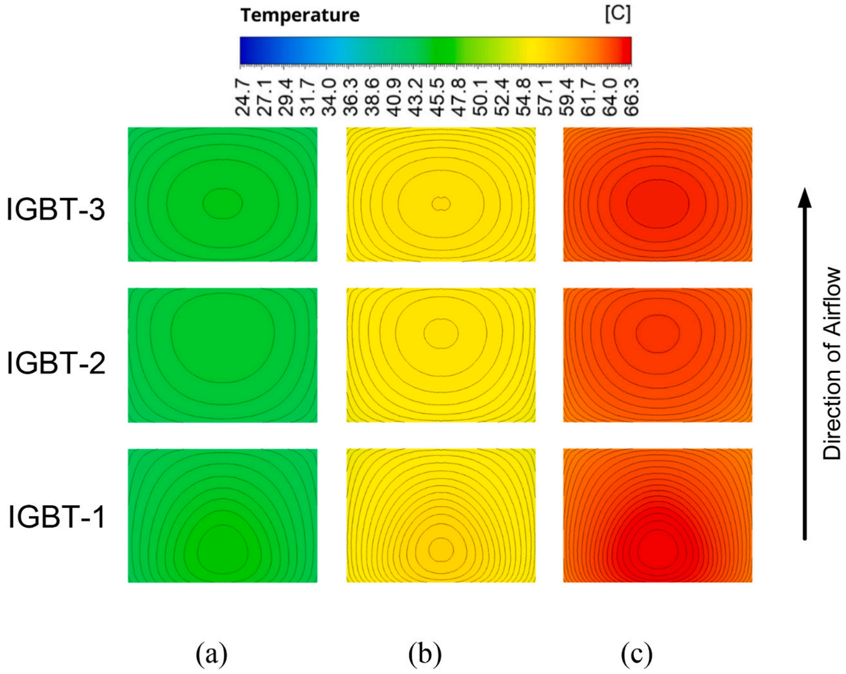

Fig. 12. Temperature distribution showing thermal gradient within the IGBTs' surface in the model with optimised V-shaped cut (ε = 0.255pu). Heat flux per IGBT module: (a) 50W; (b) 80W; (c) 100W.

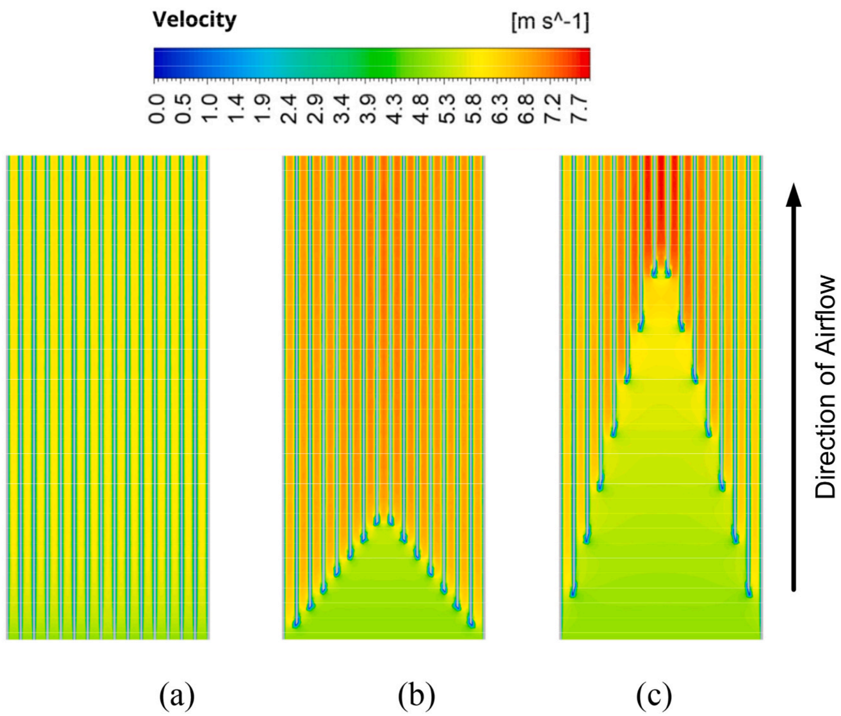

Fig. 13. Contours of velocity magnitude for V-shaped cut (a) ε = 0pu, (b) ε = 0.255pu, and (c) ε = 0.83pu.

Fig. 12 illustrates the simulation results of the temperature distribution across the surface area of the semiconductors installed on the modified heat sink with the optimal V-shaped cut value of 0.255 pu. It can be observed that the temperature gradient is reduced. For example, the temperature difference between the hottest and coolest points on the surface of IGBT-1 at a power flux of 100 W is 7.5 °C for the conventional benchmark heat sink and 6 °C for the optimised design.

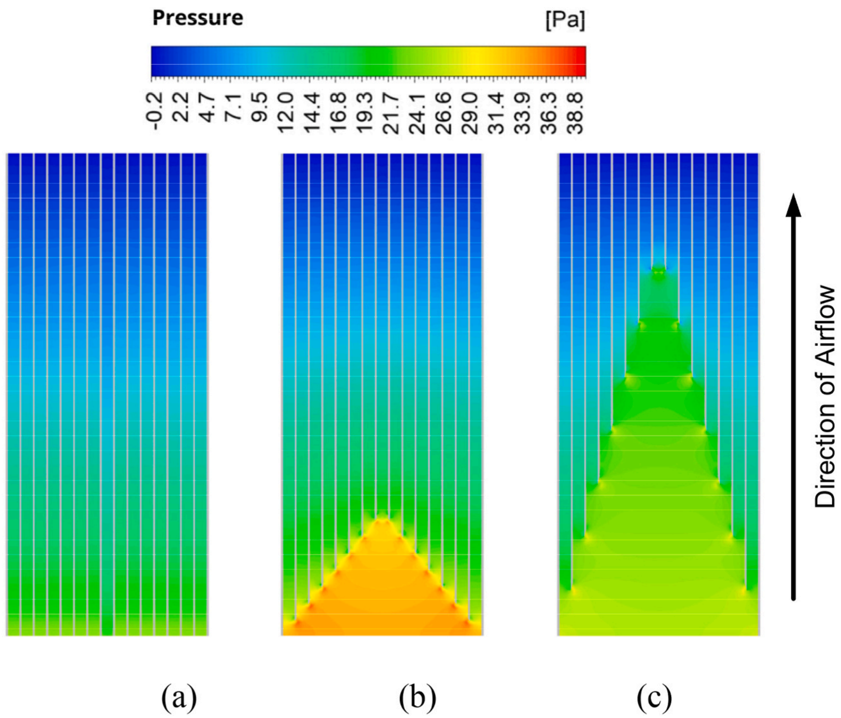

Fig. 14. Contours of static pressure for V-shaped cut (a) $\varepsilon = 0$pu, (b) $\varepsilon = 0.255$pu, and (c) $\varepsilon = 0.83$pu.

Figs. 13 and 14 present the airflow velocity and static pressure contours, respectively, for three selected V-shaped cut configurations: $\varepsilon = 0$ (benchmark), $\varepsilon = 0.255$ pu, and $\varepsilon = 0.83$ pu. As shown in Fig. 13, the average airflow velocity through the heat sink for the benchmark model ($\varepsilon = 0$) is approximately 5 m/s. However, introducing a V-shaped cut in the fins increases the velocity magnitude in the uncut regions of the heat sink, therefore, enhancing convective heat transfer and improving thermal performance in those areas. This also indicates that thermal resistance in the cut region is increased. Fig. 14 shows that the highest static pressure occurs in the V-shaped cut area of the heat sink with the optimal design, confirming the effectiveness of this configuration in balancing airflow distribution and thermal resistance.

The presence of an optimum around $\varepsilon_{OPT} = 0.255$ pu can be interpreted as the result of a balance between airflow redistribution and available fin area for convection. For small V-shape cuts ($\varepsilon \to 0$), the fin area near the inlet is almost unchanged. So, the upstream region is “over-cooled”, where the first IGBT module experiences strong convection and a relatively low surface temperature, while the downstream modules receive warmer air and reduced convective capacity. This leads to a high inter-module temperature spread, as reflected by the larger standard deviations in Table 2. As ε increases, removing fins at the inlet locally raises thermal resistance and reduces the heat removal there, deliberately allowing the first module to run hotter. At the same time, the V-shaped recess acts as a plenum that modifies the pressure field and redistributes the flow.

The velocity contours in Fig. 13 show that for the optimum $\varepsilon_{OPT} = 0.255$ pu, the air in the uncut fin channels accelerates compared with the benchmark case, enhancing convective heat transfer over the middle and outlet modules. Correspondingly, the static-pressure maps in Fig. 14 indicate a pressure rise and stronger gradient in the cut region, which drives more air through the remaining fin passages downstream. In other words, the V-shape cut sacrifices some local convection area at the inlet in order to (1) reduce over-cooling of the first module, and (2) increase the effective cooling capacity in the central and outlet sections where the air would otherwise be hotter and slower. When ε becomes too large (e.g., $\varepsilon \gg 0.3$ pu), the fin area removed at the inlet is excessive: total convective surface is substantially reduced, and the overall thermal resistance of the sink grows. So all module temperatures rise, and the benefit of improved airflow distribution is outweighed by the loss of “reserve” fin area. The minimum in temperature standard deviation observed at $\varepsilon_{OPT} = 0.255$ pu therefore represents the trade-off point at which airflow acceleration and pressure-driven redistribution are strong enough to equalise module temperatures, but the remaining fin area is still sufficient to maintain low absolute temperatures across the entire heat sink.

5. Conclusion

This paper presents an analysis of a solution aimed at improving the thermal gradient across power semiconductor modules mounted on the top surface of a conventional air-forced heat sink used in industrial power electronic applications. The proposed solution involves removing a part of the fin area at the air inlet side of the heat sink in the form of a V-shaped cut (Fig. 3). This modification introduces variable thermal resistance along the length of the heat sink reducing the temperature differences between the

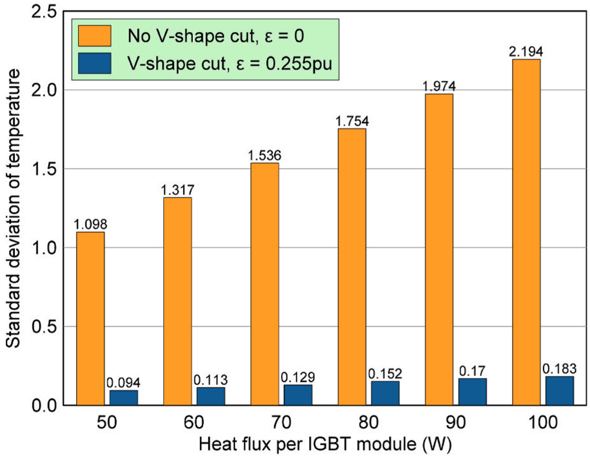

Fig. 15. The standard temperature deviation vs. heat flux per IGBT module for the benchmark heat sink (no V-shaped cut, $\varepsilon = 0$) and the model with optimised V-shaped cut ($\varepsilon = 0.255$pu).

semiconductor modules.

ANSYS software was used to perform a numerical analysis comparing the proposed design with the conventional benchmark heat sink. The standard deviation of the average temperatures across the three IGBT modules was selected as the optimisation criterion for evaluating thermal performance. The simulations were conducted under various power losses in the IGBT modules operating at steady-state conditions. The main findings of this study can be summarised as follows:

- A V-shaped cut of the fins at the airflow inlet effectively reduces temperature non-uniformity across power semiconductor modules by redistributing airflow and thermal resistance along the heat sink length in comparison to a conventional benchmark design.
- Numerical optimisation based on the standard deviation of module average temperatures identified an optimal V-shaped cut depth of $\varepsilon = 0.255$pu, which provides the minimum thermal gradient over the semiconductor surface areas. Fig. 15 compares the temperature standard deviation between proposed and benchmark designs.
- The proposed design modification represents a cost-effective solution applicable to standard heat sinks to improve the thermal performance, reliability, and lifetime of power electronic devices used in industrial applications.

As the proposed approach requires experimental validation, future work will include a series of practical tests using a heat sink with the same dimensions. These experiments will be used to experimentally validate the numerical predictions, refine the model parameters, and strengthen the practical applicability of the proposed design. Future work will also involve an investigation of the heat sink thermal performance under transient conditions and a six-module configuration, including a turbulence model sensitivity study. In addition, future work will analyse structural and manufacturing feasibility, along with robustness to dust accumulation and clogging.

CRediT authorship contribution statement

Andrew Sharp: Supervision, Methodology, Investigation, Conceptualization. **Shafiul Monir:** Validation, Supervision, Software, Project administration, Methodology, Conceptualization. **Valentine Dumeril:** Visualization, Software, Methodology, Data curation, Conceptualization. **Cedric Belloc:** Writing – review & editing, Visualization, Methodology. **Mobayode Akinsolu:** Writing – review & editing, Visualization, Methodology. **Yuriy Vagapov:** Writing – review & editing, Writing – original draft, Visualization, Methodology, Formal analysis.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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